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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

DEB, ANJAN K

ART UNIT PAPER NUMBER

2858

DATE MAILED: 03/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/776,778	BHATTACHARYA ET AL.	
	Examiner	Art Unit	
	Anjan K. Deb	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 February 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11 and 15-19 is/are rejected.
- 7) ☒ Claim(s) 12-14 and 20-22 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 February 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the “passive load connected between third terminal of transistor and a second voltage supply” (see claims 1, 15) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. (Fig. 2 shows, a passive load 204 connected between third terminal D of transistor MP1 and ground. Therefore the second supply voltage appears to be missing in this figure).

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement-drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

In addition to Replacement Sheets containing the corrected drawing figure(s), applicant is required to submit a marked-up copy of each Replacement Sheet including annotations indicating the changes made to the previous version. The marked-up copy must be clearly labeled as "Annotated Sheets" and must be presented in the amendment or remarks section that explains the change(s) to the drawings. See 37 CFR 1.121(d)(1). Failure to timely submit the proposed drawing and marked-up copy will result in the abandonment of the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Battes (US 3,760,272).

Re claim 1, Battes discloses, circuit (Figure) for indicating a voltage level of an input (1) signal V1 applied to the circuit, the circuit comprising at least one transistor (4) including a first terminal connected to a first voltage supply (+B,9,19), a second terminal for receiving the input (1) signal V1, and a third terminal coupled to an output (5,17,18) of the circuit and a passive load (17) (column 2 lines 47-52) connected between the third terminal of the transistor (4) and a second voltage supply (ground) wherein the circuit is configured to generate an output signal at the output 18 of the circuit, wherein the output signal being at a first value indicates that the

input signal is substantially at a first voltage level, and wherein the output signal being at a second value indicates that the input signal is substantially at a second voltage level (signal level detector). Since Battes discloses a signal level detector it produces an output signal indicative of the level of the input signal, therefore the output signal being at a first value indicates that the input signal is substantially at a first voltage level, and wherein the output signal being at a second value indicates that the input signal is substantially at a second voltage level is inherently disclosed.

3. Claims 1-7, 15, 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Kamiya (US 4,071,822).

Re claim 1, 15 Kamiya discloses, circuit (Fig. 3) for indicating a voltage level of an input signal (C) applied to the circuit, the circuit comprising at least one transistor (6) including a first terminal connected to a first voltage supply (10), a second terminal for receiving the input signal (C), and a third terminal coupled to an output (D) of the circuit, and a passive load (14) (column 2 lines 47-52) connected between the third terminal of the transistor (6) and a second voltage supply (15) wherein the circuit is configured to generate an output signal at the output (21,I,22,K) of the circuit, wherein the output signal being at a first value indicates that the input signal is substantially at a first voltage level, and wherein the output signal being at a second value indicates that the input signal is substantially at a second voltage level (column 4 lines 40-68, column 5 lines 1-15)(see also Fig. 4).

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Re claim 2, Kamiya discloses first voltage supply 10 is a positive voltage supply and the second voltage supply (15) is a negative voltage supply (-Vss)(column 3 line 56) with respect to the first voltage supply.

Re claim 3, Kamiya discloses buffer circuit (13, 16, 17,20) connected in series between the third terminal of the transistor 6 and the output (G,I,K) of the circuit (Fig. 3).

Re claim 4, Kamiya discloses inverter 17,20 operatively connected in series between the third terminal of the at least one transistor and the output of the circuit.

Re claim 5, Kamiya discloses passive load comprises a resistor 14 including a first terminal connected to the third terminal of the transistor 6 and a second terminal connected to the second voltage supply (15).

Re claims 6, 7, 16 Kamiya discloses PMOS and NMOS transistor (column 3 lines 5-8).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiya (US 4,071,822) in view of Bonaccio (US 5,859,461).

Re claim 8, Kamiya did not expressly disclose first voltage level is about 1.8 volts and the second voltage level is about 3.3 volts.

Bonaccio discloses method and apparatus for interfacing integrated circuits having different supply voltages including 1.8 volts and 3.3 volts, which are standard operating voltage levels of analog and digital integrated circuits.

At the time of the invention it would have been obvious for one of ordinary skill in the art to modify Kamiya by including first and second voltage level of 1.8 volts and 3.3 volts respectively as disclosed by Bonaccio for interfacing integrated circuits having different supply voltages.

6. Claims 9-11, 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiya (US 4,071,822) in view of Battes (US 3,760,272).

Re claims 9-11, 17-19 Kamiya did not expressly disclose voltage level shift circuit.

Battes discloses level shift circuit 17 (potentiometer) for adjusting tolerances in supply (reference) voltage (column 4 lines 3-5). A control signal is inherently disclosed as required for controlling potentiometer resistance.

At the time of the invention it would have been obvious for one of ordinary skill in the art to modify Kamiya by adding voltage level shift circuit disclosed by Battes connected between first voltage supply and a transistor to generate a voltage drop for adjusting tolerances in supply voltage levels.

Allowable Subject Matter

7. Claims 12-14, 20-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Claims 12-14, 20-22 are allowable for the inclusion of a second transistor, the second transistor including a first terminal connected to the first terminal of the at least one transistor, the second transistor including second and third terminals connected to the first voltage supply of the circuit in combination with remaining claims limitations.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Pommerening (US 3,409,784) discloses, circuit (Fig. 1-3) for indicating a voltage level of an input signal (A) applied to the circuit, the circuit comprising at least one transistor (2) including a first terminal connected to a first voltage supply, a second terminal for receiving the input signal (A), and a third terminal coupled to an output of the circuit and a passive load (3) connected between the third terminal of the transistor and a second voltage supply wherein the circuit is configured to generate an output signal at the output (B) of the circuit.


Takeshima (US 6,236,243 B1) discloses voltage level detection circuit comprising inverter outputs (1,0) corresponding to first and second input voltage level.

Schreck (US 5,170,077) discloses voltage level detecting circuit comprising transistor coupled to a load and an output (Fig. 2,3).

Bales (US 6,639,424 B2) discloses level shift circuit (Fig. 2) comprising transistor receiving a control signal having input in a first voltage range to produce an output which transitions in a second voltage range.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Anjan K. Deb whose telephone number is 571-272-2228. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lefkowitz Edwards can be reached at 571-272-2180.



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3/16/05

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